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(54) **MOS-gated power device having extended trench and doping zone and process for forming same**

(57) A trench MOS-gated device comprises a doped monocrystalline semiconductor substrate that includes an upper layer and is of a first conduction type. An extended trench in the upper layer of the substrate has a bottom portion filled with a dielectric material that forms a thick layer in the bottom of the trench. The upper portion of the trench is lined with a dielectric material and substantially filled with a conductive material, the filled upper portion of the trench forming a gate region. An extended doped zone of a second opposite conduction type extends from the upper surface into the upper layer on one side of the trench, and a doped well region of the second conduction type overlying a drain zone of the first conduction type is disposed in the upper layer on the opposite side of the trench. The drain zone is substantially insulated from the extended zone by the thick dielectric layer in the bottom portion of the trench. A heavily doped source region of the first conduction type and a heavily doped body region of the second conduction type is disposed in the well region at the upper surface of the upper layer. An interlevel dielectric layer is disposed on the upper surface overlying the gate and source regions, and a metal layer overlying the upper surface and the interlevel dielectric layer is in electrical contact with the source and body regions and the extended zone.

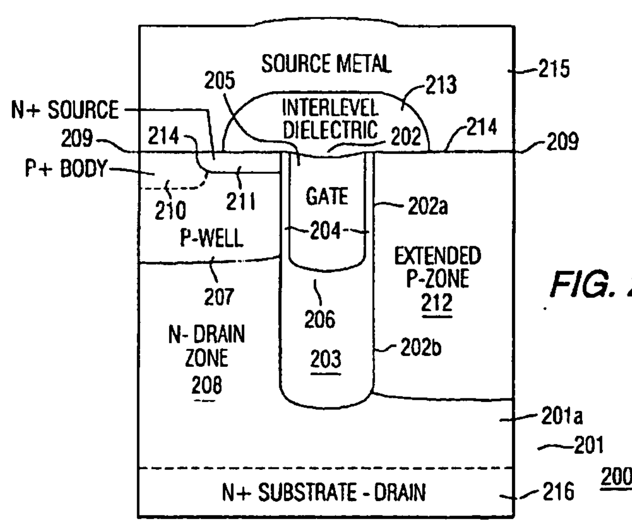

FIG. 2

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Description

[0001] The present invention relates to semiconductor devices and, in particular, to a trench MOS-gated power device having an extended doped zone separated from a drain zone by an extended trench.

[0002] An MOS transistor having a trench gate structure offers important advantages over a planar transistor for high current, low voltage switching applications. The DMOS trench gate includes a trench extending from the source to the drain and having sidewalls and a floor that are each lined with a layer of thermally grown silicon dioxide. The lined trench is filled with doped polysilicon. The structure of the trench gate allows less constricted current flow and, consequently, provides lower values of specific on-resistance. Furthermore, the trench gate makes possible a decreased cell pitch in an MOS channel extending along the vertical sidewalls of the trench from the bottom of the source across the body of the transistor to the drain below. Channel density is increased, which reduces the contribution of the channel to on-resistance. The structure and performance of trench DMOS transistors are discussed in Bulucea and Rossen, "Trench DMOS Transistor Technology for High-Current (100 A Range) Switching," in Solid-State Electronics, 1991, Vol. 34, No. 5, pp 493-507, the disclosure of which is incorporated herein by reference. In addition to their utility in DMOS devices, trench gates are also advantageously employed in insulated gate bipolar transistors (IGBTs), MOS-controlled thyristors (MCTs), and other MOS-gated devices.

[0003] FIG. 1 schematically depicts the cross-section of a trench-gated N-type MOSFET device 100 of the prior art formed on an upper layer 101a of an N+ substrate 101. Device 100 includes a trench 102 whose sidewalls 103 and floor 104 are lined with a gate dielectric such as silicon dioxide. Trench 102 is filled with a conductive material 105 such as doped polysilicon, which serves as an electrode for gate region 106.

[0004] Upper layer 101a of substrate 101 further includes P-well regions 107 overlying an N-drain zone 108. Disposed within P-well regions 107 at an upper surface 109 of upper layer 101a are heavily doped P+ body regions 110 and heavily doped N+ source regions 111. An interlevel dielectric layer 112 is formed over gate region 106 and source regions 111. Contact openings 113 enable metal layer 114 to contact body regions 110 and source regions 111. The rear side 115 of N+ substrate 101 serves as a drain.

[0005] Although FIG. 1 shows only one MOSFET, a device currently employed in the industry consists of an array of them arranged in various cellular or stripe layouts. As a result of recent semiconductor manufacturing improvements enabling increased densities of trench gated devices, the major loss in a device when in a conduction mode occurs in its lower zone, i.e., increased drain resistivity. Because the level of drain doping is typically determined by the required voltage blocking capability, increased drain doping for reducing resistivity is not an option. Thus, there is a need for reducing the resistivity of the drain region in a semiconductor device without also reducing its blocking capability. The present invention meets this need.

[0006] The present invention includes a trench MOS-gated device comprising a substrate including an upper layer, said substrate comprising doped monocrystalline semiconductor material of a first conduction type, an extended trench in said upper layer, said trench having a bottom portion filled with a dielectric material, said material forming a thick dielectric layer in said bottom of said trench, said trench further having an upper portion lined with a dielectric material and substantially filled with a conductive material, said filled upper portion of said trench forming a gate region, characterized in that a doped extended zone of a second opposite conduction type extending from an upper surface into said upper layer on one side of said trench, a doped well region of said second conduction type overlying a drain zone of said first conduction type in said upper layer on the opposite side of said trench, said drain zone being substantially insulated from said extended zone by said thick dielectric layer in said bottom portion of said trench, a heavily doped source region of said first conduction type and a heavily doped body region of said second conduction type disposed in said well region at said upper surface, an interlevel dielectric layer on said upper surface overlying said gate and source regions; and a metal layer overlying said upper surface and said interlevel dielectric layer, said metal layer being in electrical contact with said source and body regions and said extended zone.

[0007] Advantageously, a trench MOS-gated device that comprises a doped monocrystalline semiconductor substrate that includes an upper layer and is of a first conduction type. An extended trench in the substrate has a bottom portion filled with a dielectric material that forms a thick layer in the bottom of the trench. The upper portion of the trench is lined with a dielectric material and substantially filled with a conductive material, the filled upper portion of the trench forming a gate region.

[0008] An extended doped zone of a second opposite conduction type extends from an upper surface into the upper layer of the substrate on one side of the trench, and a doped well region of the second conduction type overlying a drain zone of the first conduction type is disposed in the upper layer on the opposite side of the trench. The drain zone is substantially insulated from the extended zone by the thick dielectric layer in the bottom portion of the trench.

[0009] A heavily doped source region of the first conduction type and a heavily doped body region of the second conduction type is disposed in the well region at the upper surface of the upper layer. An interlevel dielectric layer is disposed on the upper surface overlying the gate and source regions, and a metal layer disposed on the upper surface of the upper layer and the interlevel die-

lectric layer is in electrical contact with the source and body regions and the extended zone.

[0010] The invention also includes a process for forming a trench MOS-gated device, said process comprising forming an extended trench in an upper layer of a substrate, said substrate comprising doped monocrystalline semiconductor material of a first conduction type, substantially filling said extended trench with a dielectric material, characterized by selectively implanting and diffusing a dopant of a second opposite conduction type into said upper layer on one side of said extended trench, thereby forming an extended zone extending from an upper surface into said upper layer, layer removing a selected portion of said dielectric material from an upper portion of said trench, leaving a thick dielectric layer in a bottom portion of said trench, forming sidewalls comprising dielectric material on the upper portion of said trench and substantially filling said upper portion with a conductive material, thereby forming a gate region in said upper portion of said trench, forming a doped well region of said second conduction type in said upper layer on the side of said trench opposite said extended zone, forming a heavily doped source region of said first conduction type and a heavily doped body region of said second conduction type in said well region at said upper surface, forming an interlevel dielectric layer on said upper surface overlying said gate and source regions, forming a metal layer overlying said upper surface and said interlevel dielectric layer, said metal layer being in electrical contact with said source and body regions and said extended zone, and forming a doped drain zone of said first conduction type extending beneath said well region and said extended zone.

[0011] Conveniently, a process for constructing a trench MOS-gated device that comprises forming an extended trench in an upper layer of a doped monocrystalline semiconductor substrate of a first conduction type, and substantially filling the trench with a dielectric material. A dopant of a second opposite conduction type is implanted and diffused into the upper layer on one side of the extended trench, thereby forming a doped extended zone extending into the upper layer from its upper surface.

[0012] A selected portion of the dielectric material is removed from an upper portion of the trench, leaving a thick dielectric layer in its bottom portion. Sidewalls comprising dielectric material are formed in the upper portion of the trench, which is then substantially filled with a conductive material, thereby forming a gate region in the upper portion of the trench.

[0013] A doped well region of the second conduction type is formed in the upper layer of the substrate on the side of the trench opposite the doped extended zone. A heavily doped source region of the first conduction type and a heavily doped body region of the second conduction type are formed in the well region at the upper surface of the upper layer. An interlevel dielectric layer is deposited on the upper surface overlying the gate and source regions, and a metal layer is formed over the upper surface and the interlevel dielectric layer, the metal layer being in electrical contact with the source and body regions and the extended zone.

[0014] The invention will also be discussed, by way of example, with reference to the accompanying drawings in which:

[0015] FIG. 1 schematically depicts a cross-section of a trench MOS-gated device 100 of the prior art.

[0016] FIG. 2 is a schematic cross-sectional representation of a trench MOS-gated device 200 of the present invention.

[0017] FIGS. 2A-D schematically depict a process for forming device 200 of the present invention.

[0018] In FIG. 2 is schematically depicted the cross-section of an MOS-gated power device 200 of the present invention. In an upper layer 201a of a substrate 201 is constructed an extended trench 202 that is partially filled with dielectric material 203. The upper portion 202a of extended trench 202 is lined with dielectric sidewalls 204 and filled with conductive material 205. Dielectric material 203 and sidewalls 204 can be silicon dioxide, and conductive material 205 can be doped polysilicon. Conductive material 205 insulated by dielectric material 203 and sidewalls 204 serves as an electrode for a gate region 206 in the upper portion of extended trench 202.

[0019] On one side of extended trench 202 is a P-well region 207 overlying an N-drain zone 208. Disposed within P-well region 207 at upper surface 209 is a heavily doped P+ body region 210 and a heavily doped N+ source region 211. On the other side of extended trench 202 is an extended P-zone 212. Extended trench 202 separates extended zone 212 from drain zone 208, which are of opposite conduction types. An interlevel dielectric layer 213 is formed over gate region 206, source region 211, and extended P-zone 212. Contact openings 214 enable metal layer 215 to contact body and source regions 210 and 211, respectively. The rear side 216 of substrate 201 serves as a drain.

[0020] Extended P-zone 212 serves to deplete charge when blocking voltage is applied, allowing a much higher conductivity material to be used for drain construction and thereby reducing the on-resistance of the device and improving its efficiency. Dielectric material 203 in lower trench portion 202b, which can beneficially be narrower than upper trench portion 202a, prevents lateral diffusion of dopants from extended P-zone 212 into N-drain zone 208. Extended P-zone 212, which is thus self-aligned with gate region 206, is shorted to source region 211 by metal layer 215. Self-alignment allows the use of structure 200 for making high density devices with blocking voltage capabilities well below 100 V. Since dielectric material 203 serves only as a barrier to dopant diffusion, its quality is not important to the performance of device 200, which would still function even if zones 208 and 212 were electrically shorted through dielectric material 203. When device 200 is in

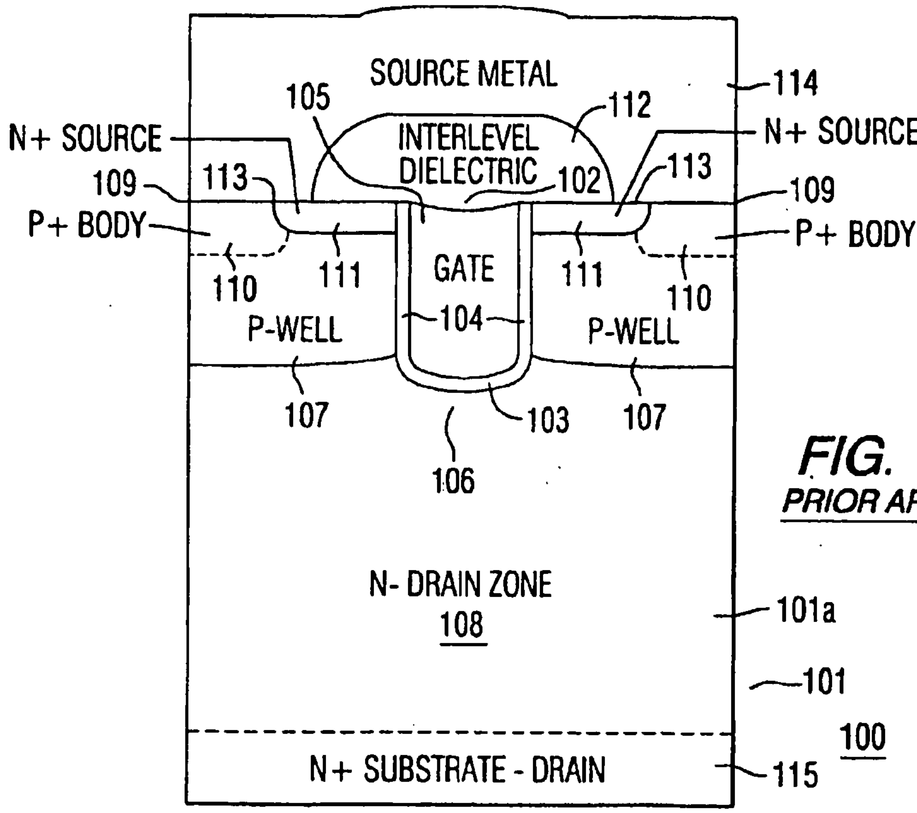

FIG. 1
PRIOR ART

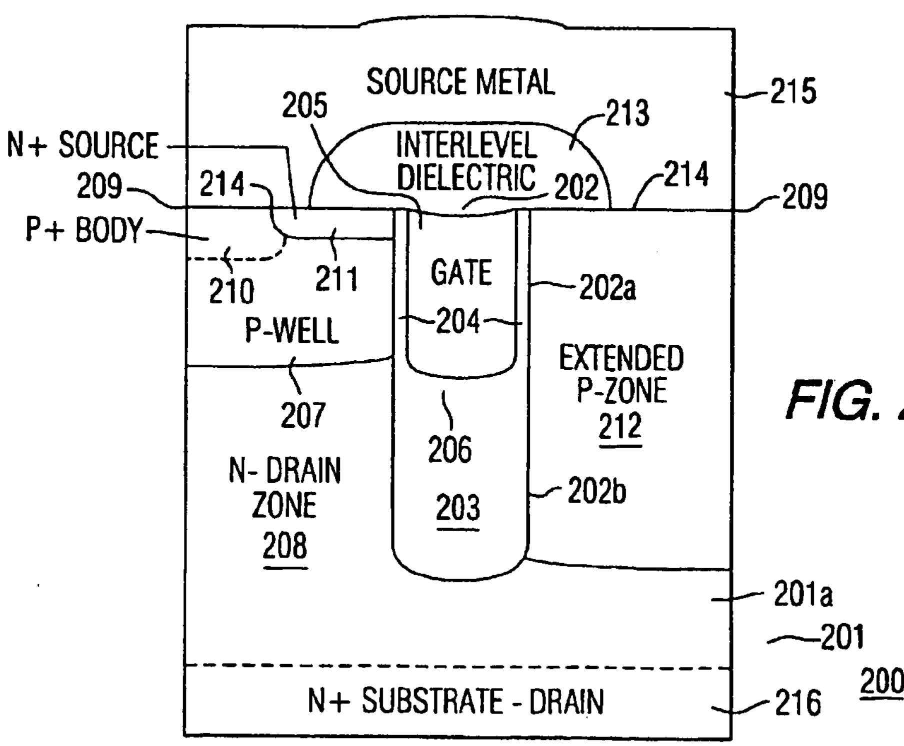

FIG. 2

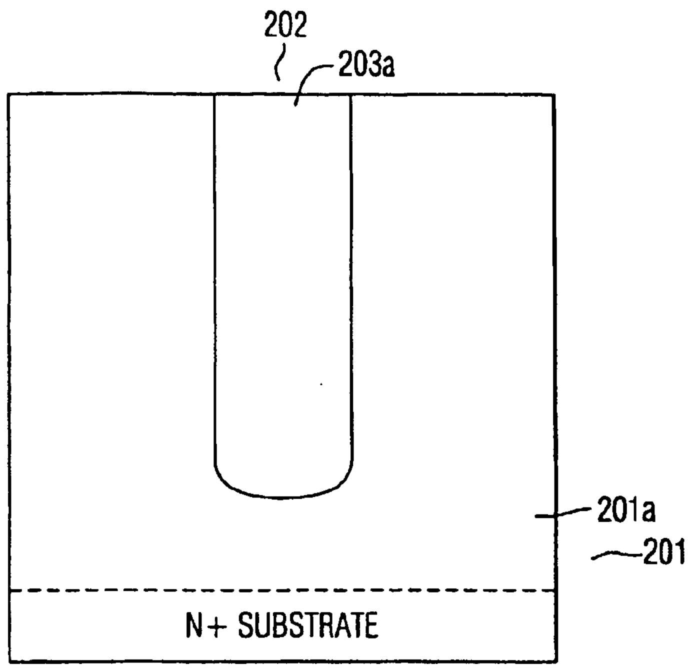
202
203a
201a
201
N+ SUBSTRATE

FIG. 2A

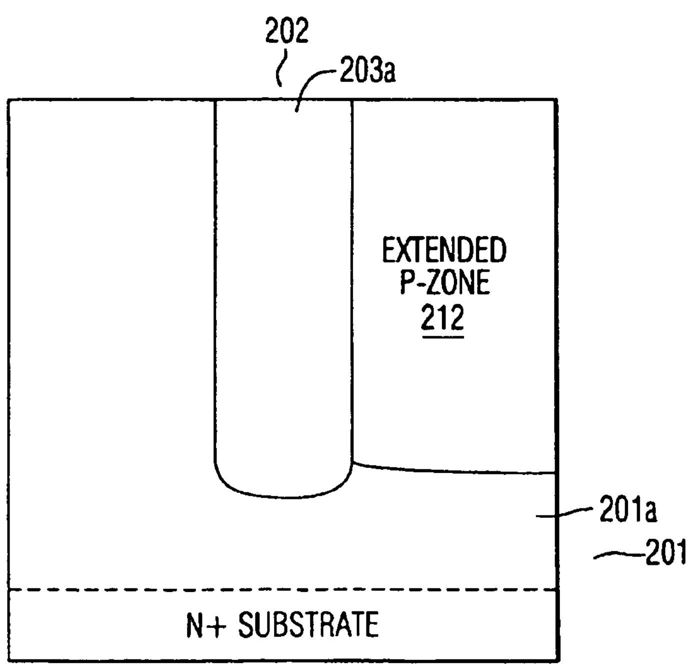
202
203a
EXTENDED
P-ZONE
212
201a
201
N+ SUBSTRATE

FIG. 2B

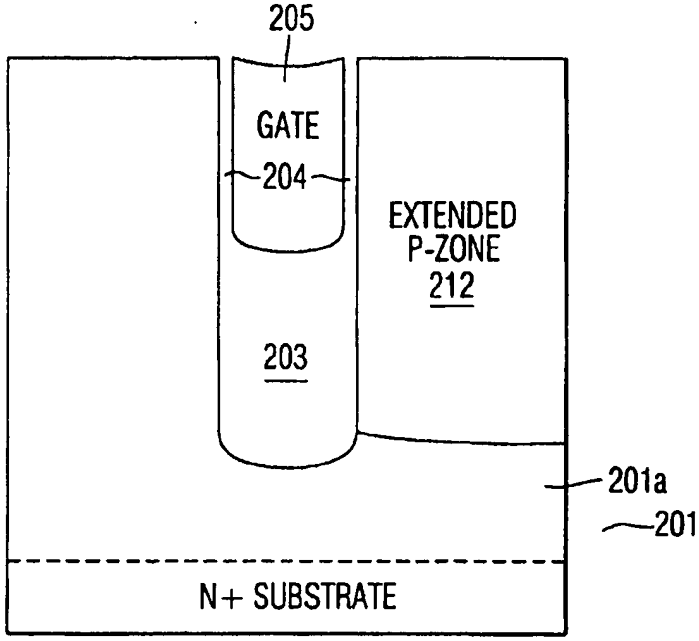
205
GATE
204
EXTENDED
P-ZONE
212
203
201a
201
N+ SUBSTRATE

FIG. 2C

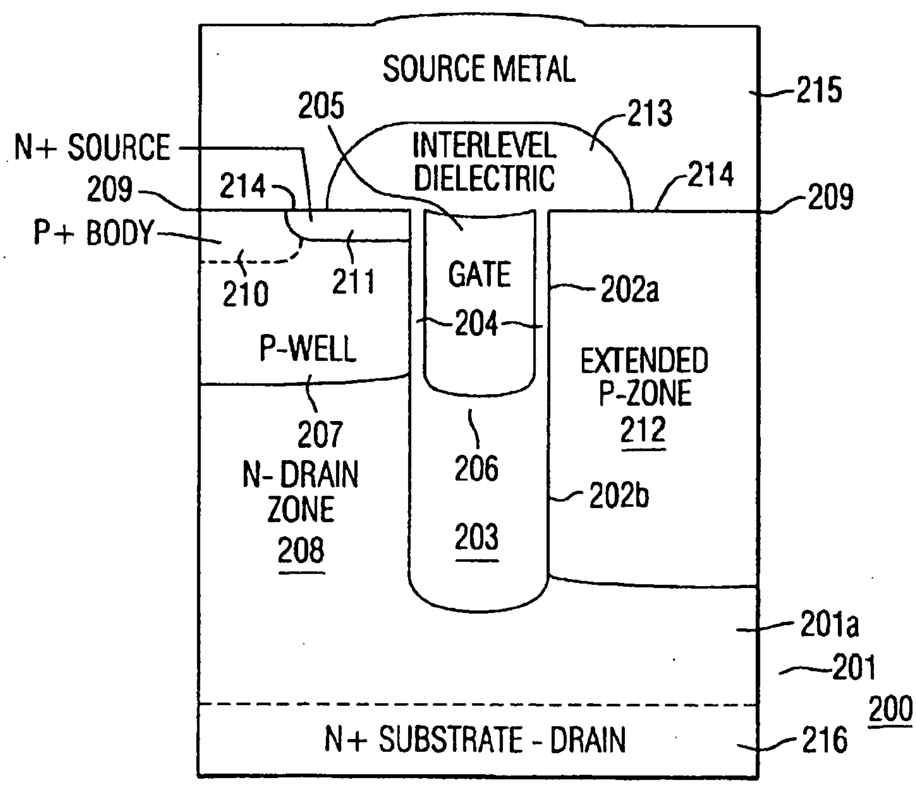
SOURCE METAL
215
205
213
N+ SOURCE
INTERLEVEL
DIELECTRIC
209
214
214
209
P+ BODY
GATE
210
211
202a
204
P-WELL
EXTENDED
P-ZONE
212
207
206
N- DRAIN
ZONE
208
202b
203
201a
201
200
N+ SUBSTRATE - DRAIN
216

FIG. 2D